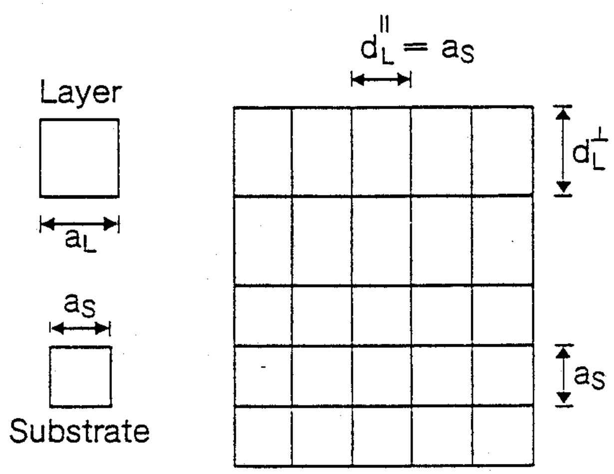
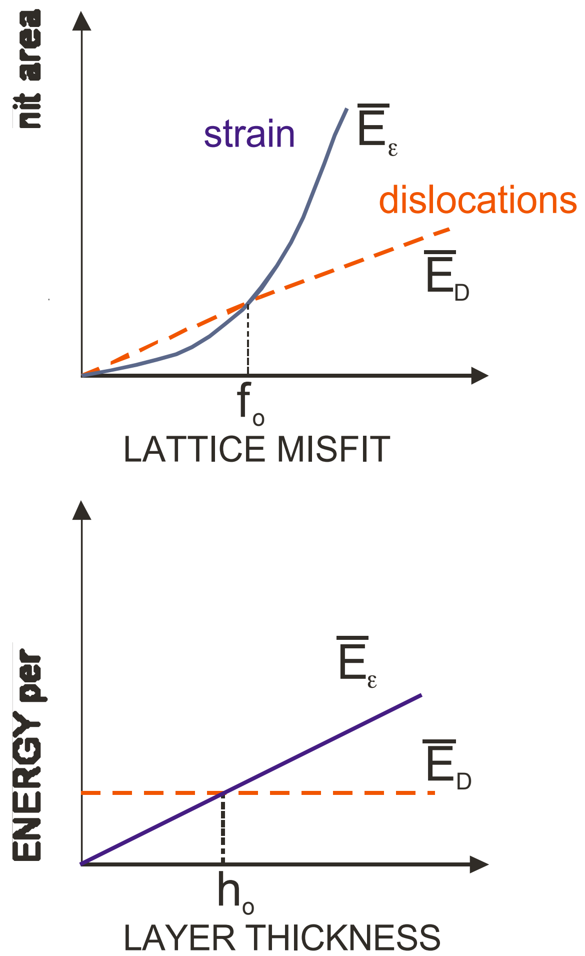
CRITICAL THICKNESS and DISLOCATIONS

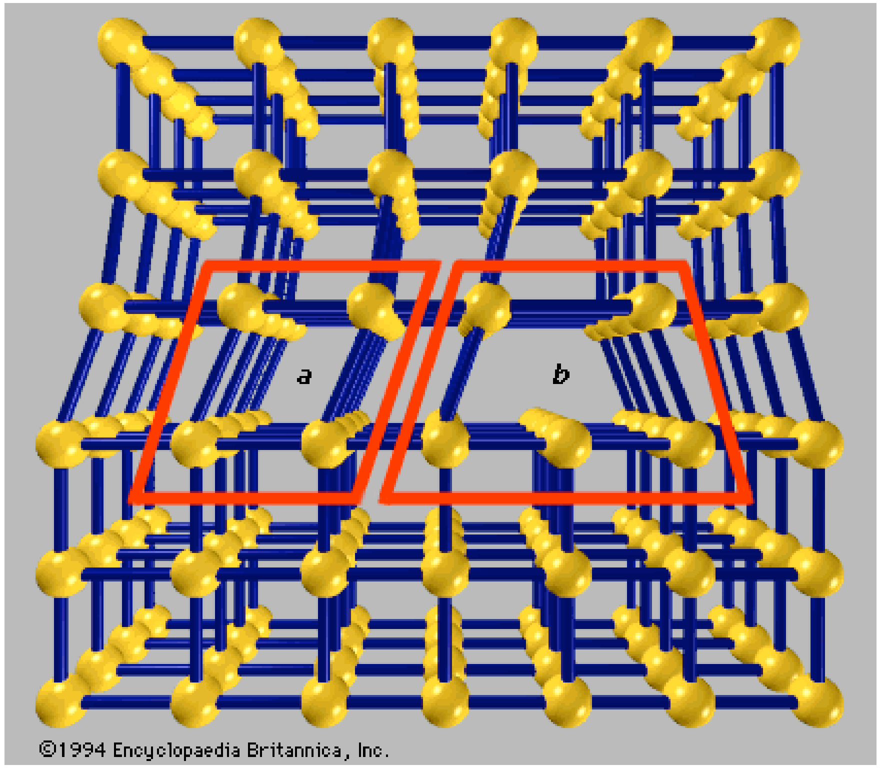
- ✓ beyond a critical lattice misfit f_0 the adjustement of the two lattices by dislocations is energetically more favorable than by strain
- ✓ for thicknesses exceeding the critical thickness h_0 dislocations are energetically more favorable than strain





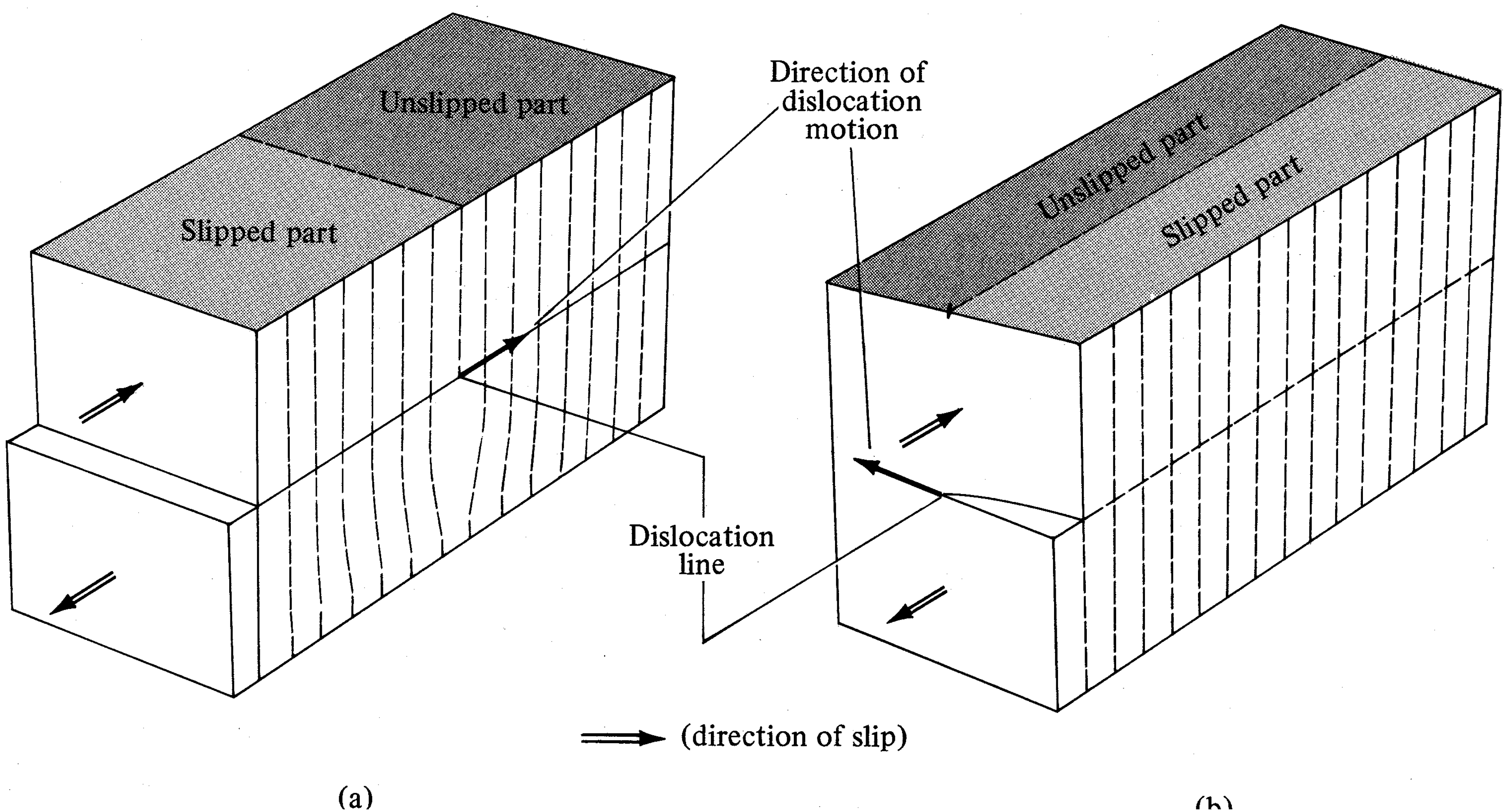
$$f_i = \frac{a_{si} - a_{oi}}{a_{oi}} \quad , \quad \varepsilon_i = \frac{a_{oi}^{str} - a_{oi}}{a_{oi}} \quad , \quad i = x, y$$

Line defects: dislocations



Edge dislocation: this line defect occurs when there is a missing row of atoms. The crystal arrangement is perfect on the top and on the bottom. The defect is the row of atoms missing from region *b*. This mistake runs in a line that is perpendicular to the page and places a strain on region *a*.

Screw dislocations

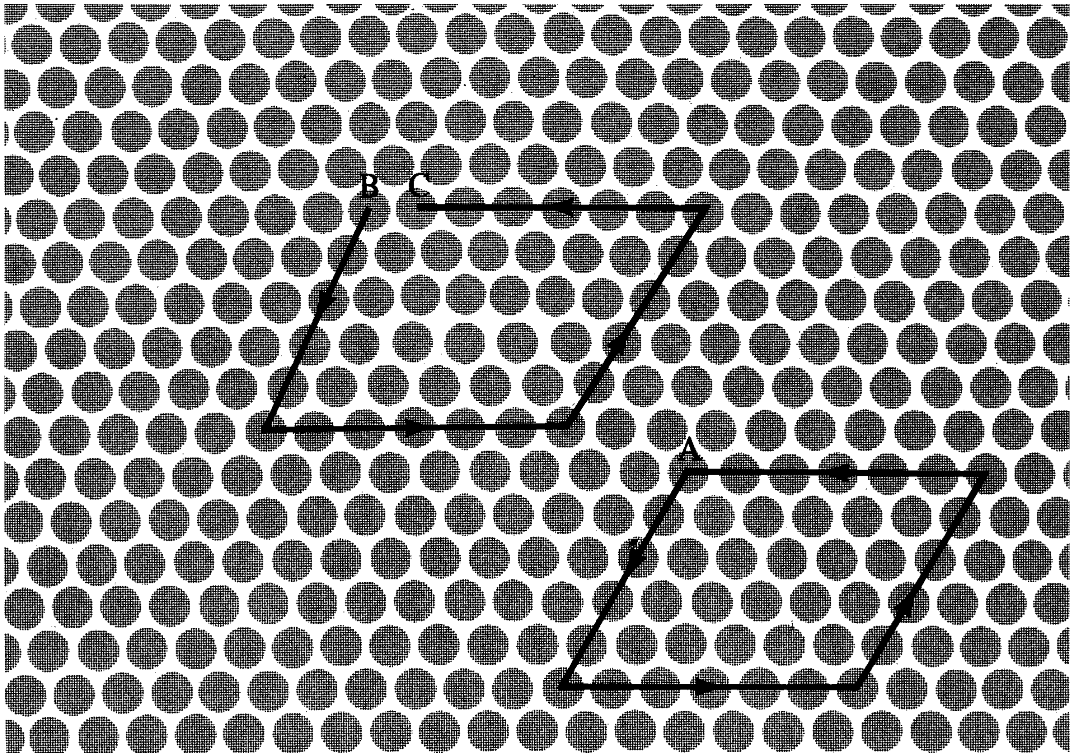


The screw dislocation can be constructed by imaging a plane terminating at the dislocation line, above which the crystal has been displaced by a lattice vector parallel to the line.

Dislocation properties

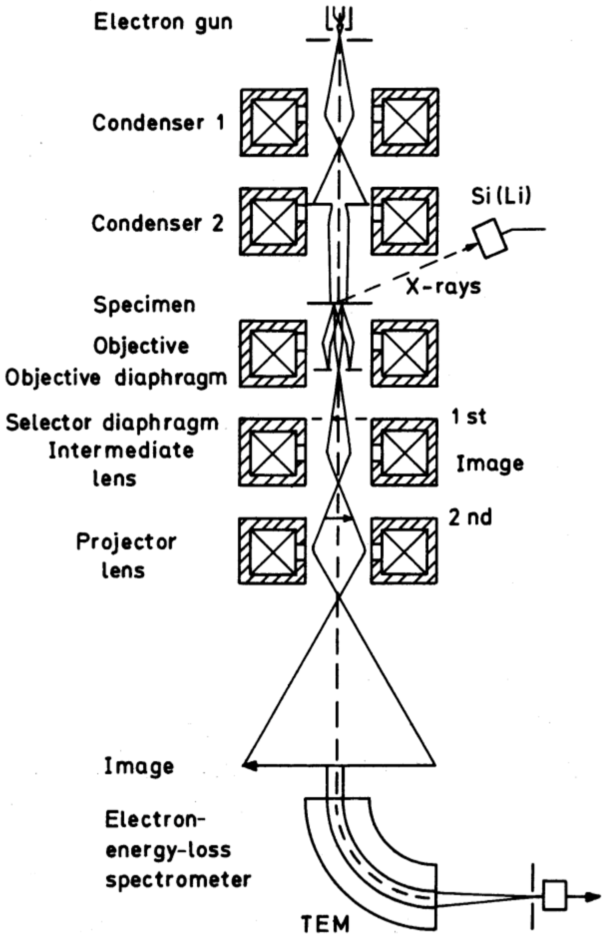
The dislocation is any linear region in the crystal with the following properties:

1) Away from the region, the crystal is locally only negligibly different from the perfect crystal.
2) In the neighborhood the region the atomic positions are substantially different from the original crystalline sites.
3) There exists a nonvanishing Burgers vector.



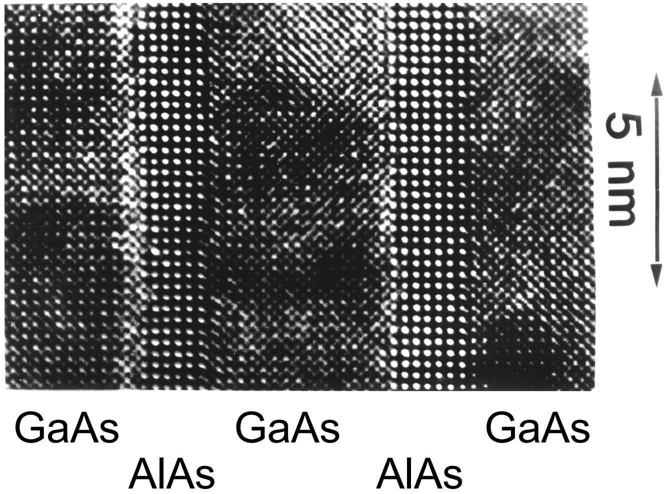
Defect Visualization- TEM

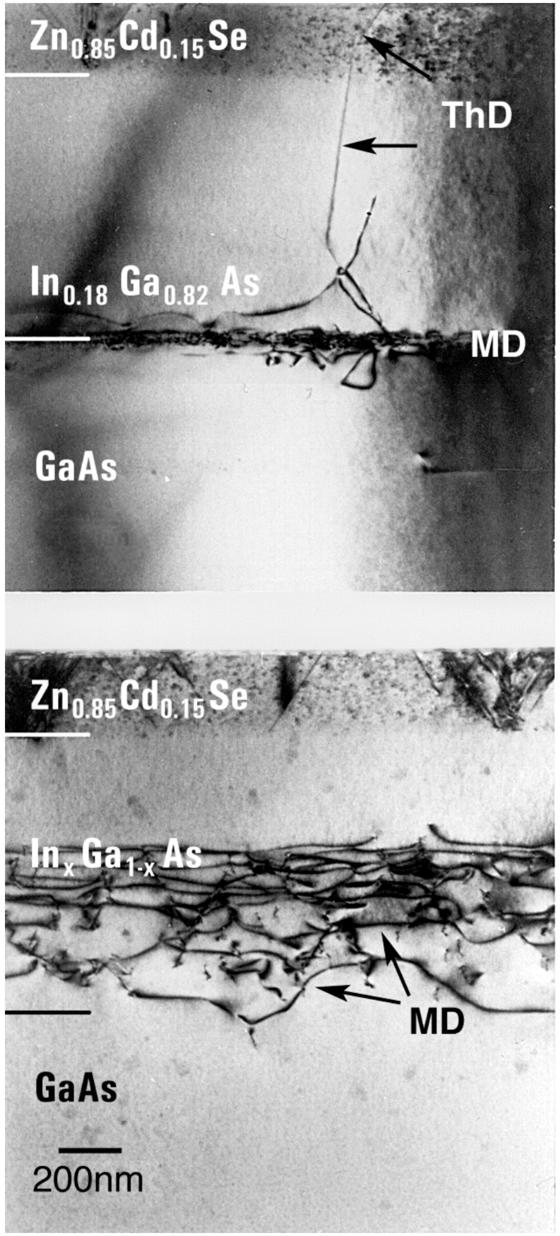
Trasmission Electron Microscope



TEM

A.Förster (MBE), D.Gerthsen (HRTEM)



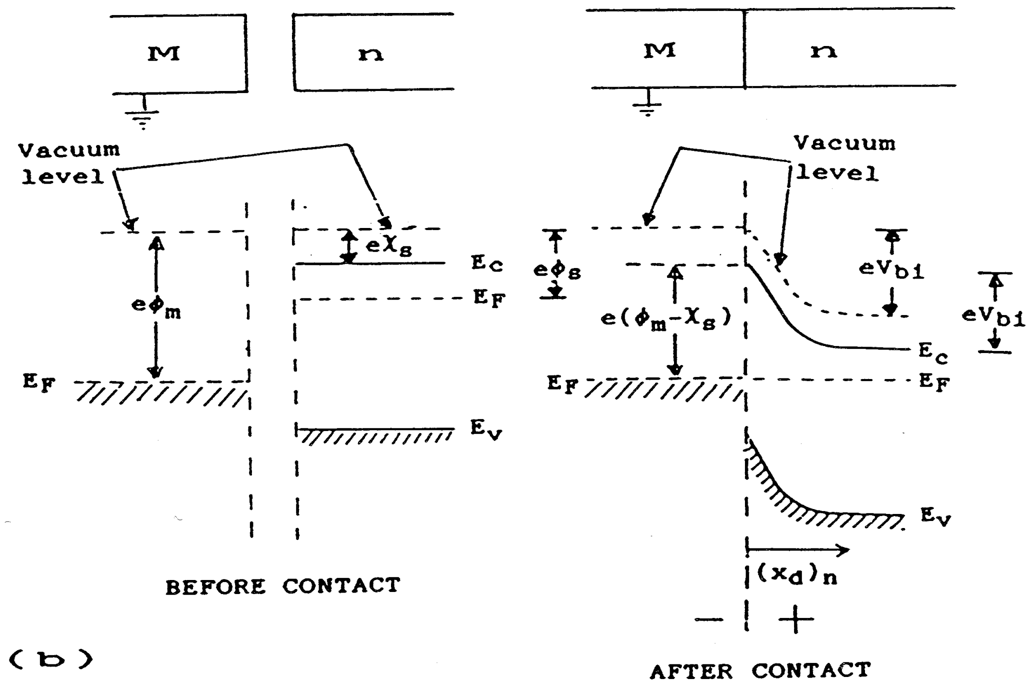


Metal-semiconductor junction

Deep Level Transient Spectroscopy (DLTS) is a powerfull method for determining the concentration of deep carrier traps in semiconductor materials.

Capacitance methods for characterization of semiconductors depend largely on the properties of metal- semiconductor junction.

x_d is the depletion thickness and depends from N_d (N_a) and V_{bi} .

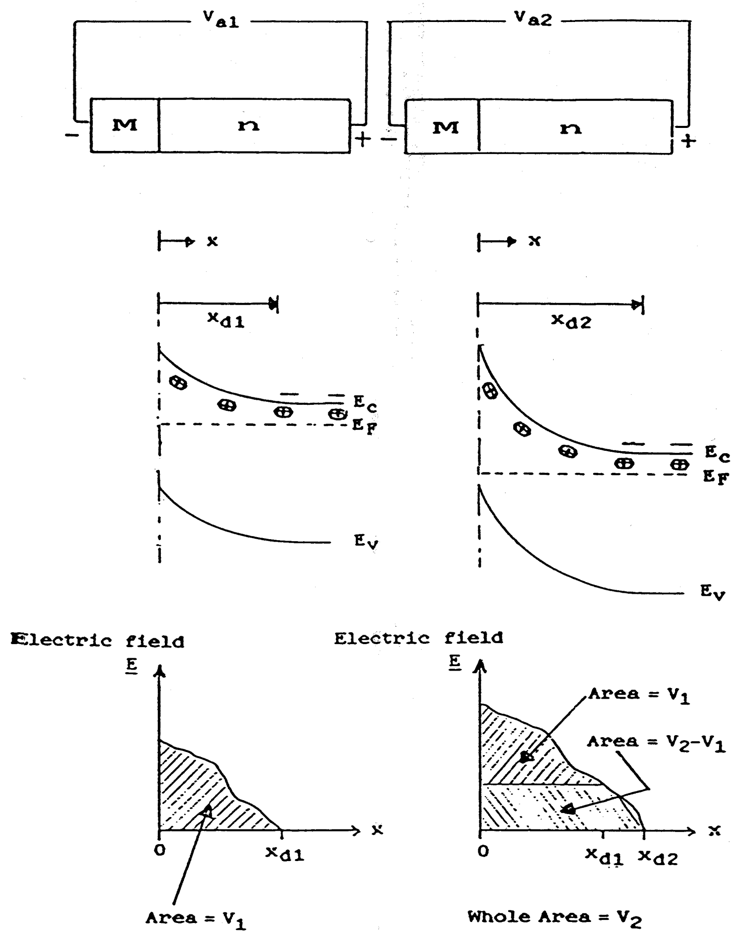


Metal-junction with reverse bias

By applying different reverse-bias voltage the depletion distance will change. In particular by increasing the applied voltage the depletion distance (x_d) will increase due to negative charge mouvement into the positive terminal of the external circuit.

Therefore this junction acts as an electrical capacitor, of capacitance $C=Q/V_a$, where Q is the charge stored in the depletion region. By changing x_d the capacitance will also change ($C=\varepsilon A/x_d$).

Va1<Va2



Semiconductors with traps

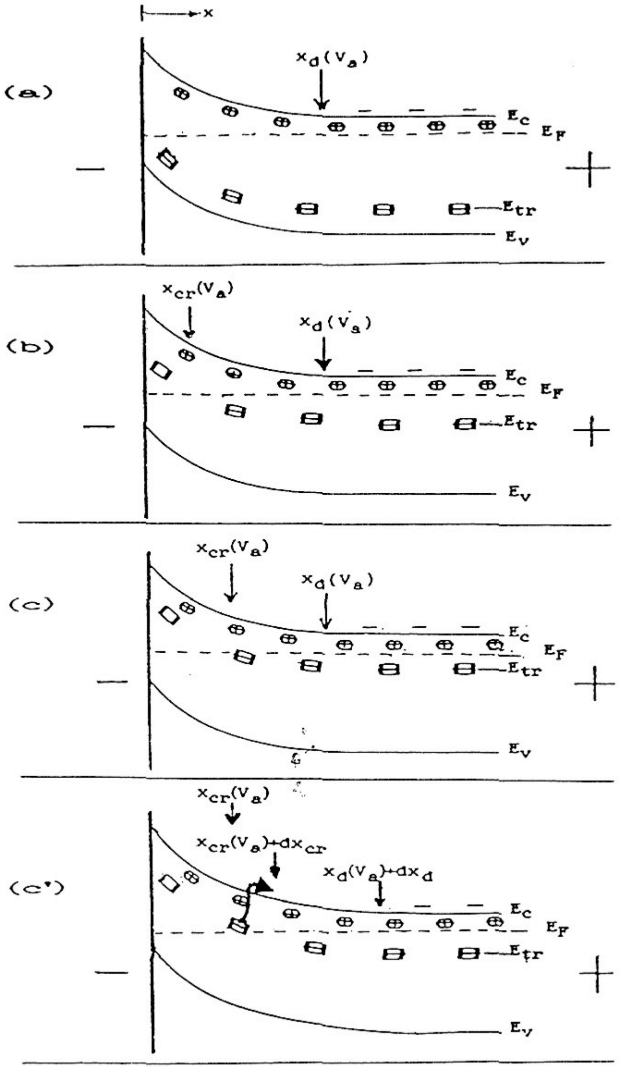
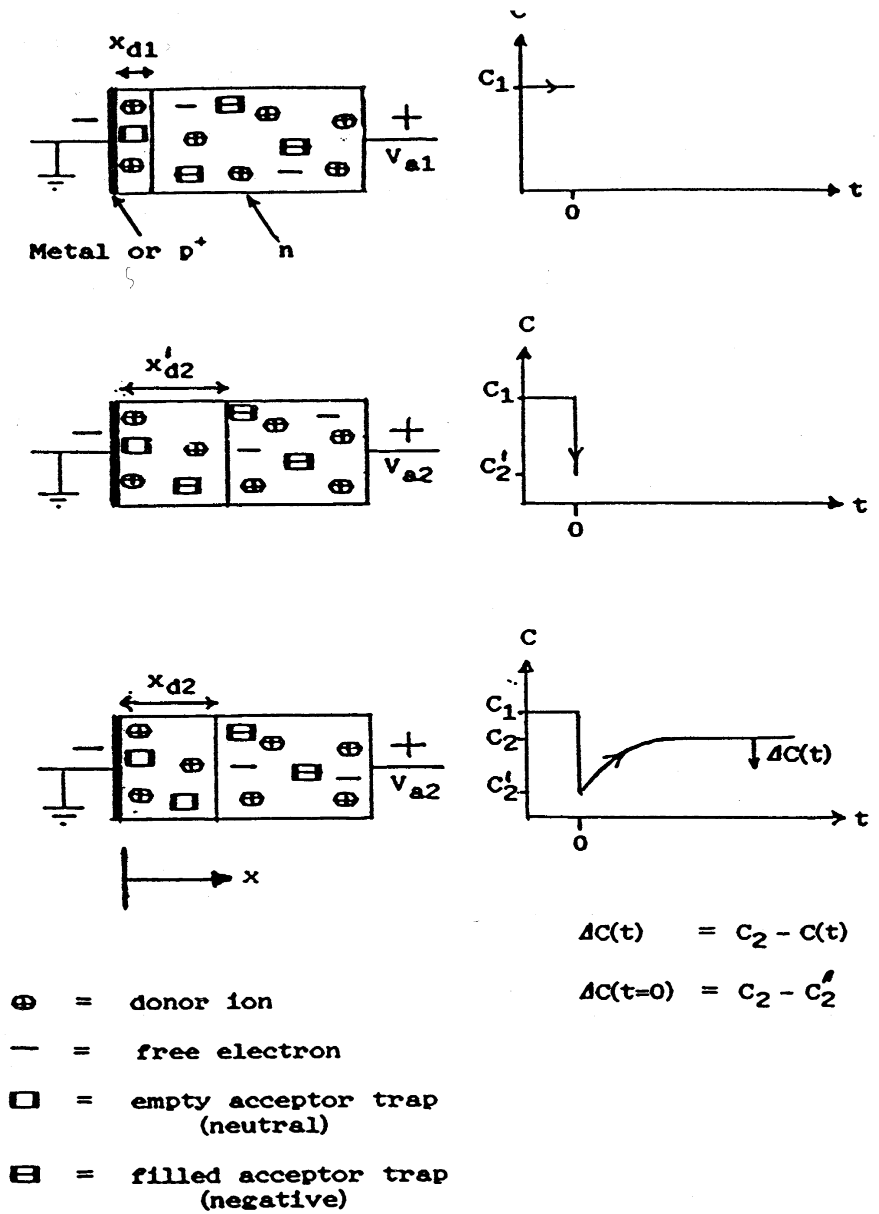


Figure 6. Electron energies as functions of distance x for materials containing acceptor-type electron-trapping levels E_{tr}. Between (c) and (c'), the applied reverse bias has been slightly increased, and traps in the spatial interval x_{cr} to $(x_{cr} + dx_{cr})$ then emit electrons to the conduction band.

$$n(x_d) = N_d(x_d) - N_{tr}(x_d)$$

Traps filled are negative

Capacitance transients



If a reverse V_{a1} is applied the depletion region is x_{d1}. Traps in the x_{d1} region are empty and the capacitance is C_1.
For $x > x_{d1}$ the traps are filled.

By increasing the reverse bias to V_{a2} the depletion region increases to x'_{d2} and the consequence is the capacitance goes to C'_2.
However the electrons on the traps in the spatial region between x_{d1} and x'_{d2} thermal equilibrium are not longer at (because free electrons have been removed from there), and thermally induced electron-emission from the traps to the conduction band begins to occur. Because this causes the space charge in the new part of the depletion region to increase from $e(N_d-N_{tr})$ towards eN_d then increases to C_2.

DLTS vs t

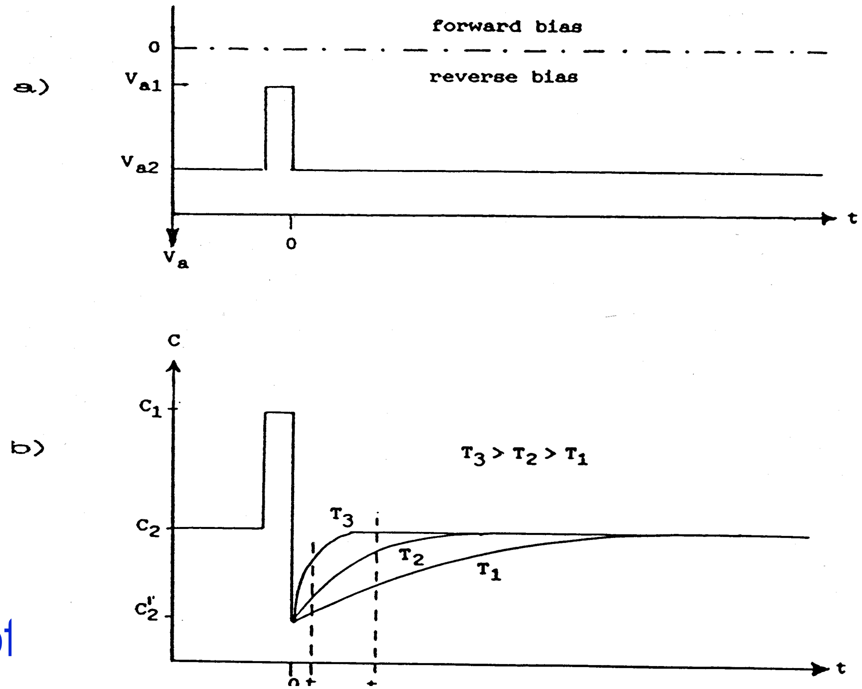
The overall effect is that a capacitance transient $\Delta C(t)$ has been produced of time dependence that is characteristic of the release of electrons from the traps:

$$\Delta C(t) = C_2 - C(t) = \Delta C(t=0)\exp\left(-\frac{t}{\tau_e}\right)$$

$$\text{with } \tau_e = (e_n)^{-1}$$

$$e_n = \sigma_n v_{th} N_c \exp\left(-\frac{(E - E_{tr})}{kT}\right)$$

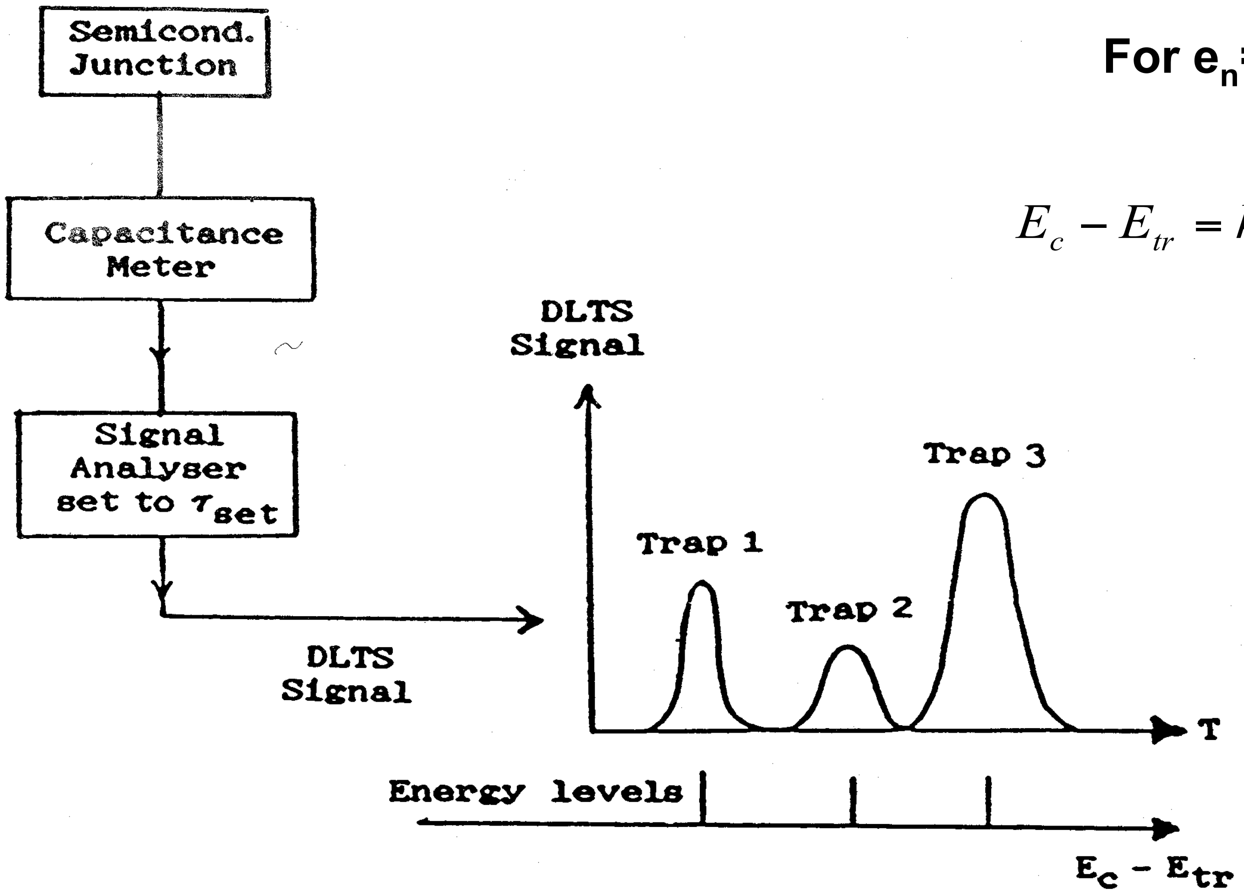
$$\Delta C(t=0)/C_2 = 0.5 N_{tr}/N_d$$



where e_n is the rate of electron emission from the traps, vth is the mean velocity of the conduction electrons.

The number of electrons or holes released from the traps per second depends on the temperature, and decays exponentially with time as the traps become progressively empty. Measurements of the decay time as a function of T allows to determine the transition energy $(E-E_{tr})$.

DLTS Measurements



For $e_n = \tau_{set}^{-1}$

$$E_c - E_{tr} = kT \ln(\tau_{set} \sigma_n v_{th} N_c)$$

At fixed T we observe a maximum in the DLTS signal when the trap emission time is equal to τ_{set} of the signal analyser.

DLTS Spectra fro MBE-n-GaAs

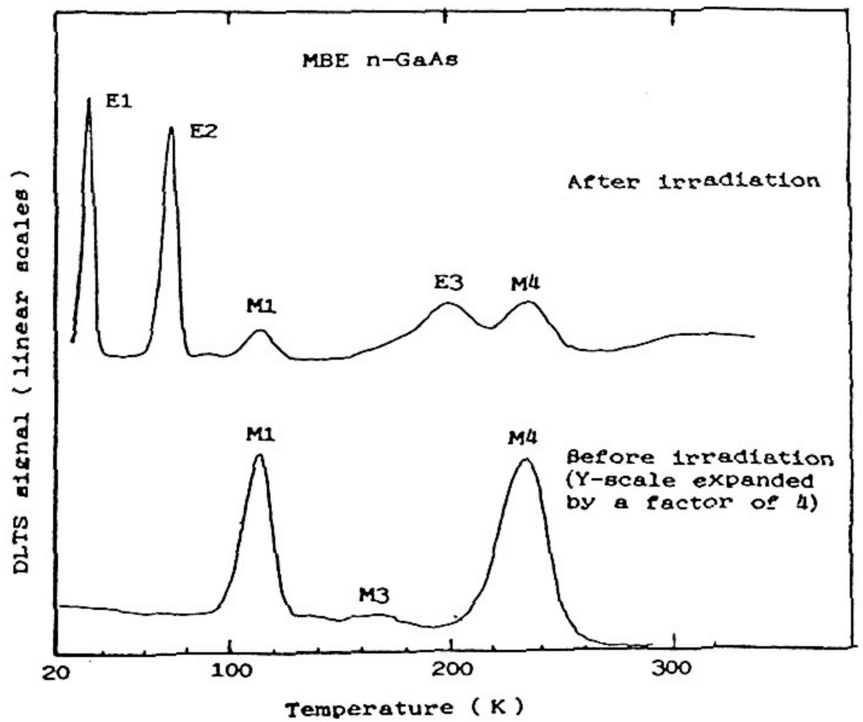


Figure 15. Majority-carrier DLTS spectra (τ_{set} = 17ms) for MBE n-GaAs before and after irradiation with 1.0 MeV protons at 293K to a dose of 1.86×10^{12} $H^{+}cm^{-2}$. The M1, M3 and M4 levels are electron traps very commonly found in GaAs grown by Molecular Beam Epitaxy. The E1, E2, E3 and E4 levels are electron traps due to irradiation-induced defects. (Nandhra 1986).

Determination of Trap Energy Levels

Analysis of the change of peak temperature with τ_{set} allows E_c-E_{tr} and σ_n.

$$e_n = \sigma_n v_{th} N_c \exp\left(-\frac{(E - E_{tr})}{kT} \right)$$

Vth proportional to T1/2

Nc proportional to T3/2

Therefore $\ln(e_n/T^2)$ as a function of 1/T is expected to be straight line having a slope equal to (Ec-Etr)/k

Figure 16. Experimental data showing how the temperature of the DLTS peak for the E3 electron trap in n-GaAs depends on the signal analyser time constant τ_{set} (Rezazadeh 1983).

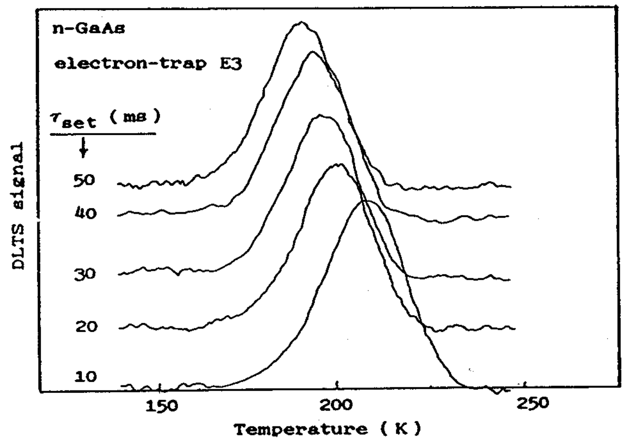


Figure 17. Arrhenius plots from DLTS data, like those of Figure 16, for the E1, E2, E3 and E4 electron traps in n-GaAs (Rezazadeh 1983).